



A Guide to VHDL

Stanley Mazor, Patricia Langstraat

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A Guide to VHDL, Second Edition is intended for the working engineer who needs to develop, document, simulate, and synthesize a design using the VHDL language. It is for system and chip designers who are working with VHDL CAD tools, and who have some experience programming in Fortran, Pascal, or C and have used a logic simulator.

A Guide to VHDL, Second Edition includes a number of paper exercises and computer lab experiments. If a compiler/simulator is available to the reader, then the lab exercises included in the chapters can be run to reinforce the learning experience. For practical purposes, this book keeps simulator-specific text to a minimum, but does use the Synopsys VHDL Simulator command language in a few cases.

A Guide to VHDL, Second Edition is designed as a primer and its contents are appropriate for an introductory course in VHDL.

The VHDL language was updated in 1992 with some minor improvements. In most cases, the language is upward compatible. Although this book is based primarily on the VHDL 1987 standard, this new second edition indicates the significant changes in the 1992 language to assist the designer in writing upwardly compatible code.

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